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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/664,856	09/19/2000	Kazuhiro Hashimoto	197372US2	5426

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EXAMINER	
HUYNH, KIM T	

ART UNIT	PAPER NUMBER
2189	7

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/664,856	Applicant(s) HASHIMOTO, KAZUHIRO	
	Examiner Kim T. Huynh	Art Unit 2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 May 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 September 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kato et al. (US Patent 6,070,205) in view of Kenny (US patent 6,393,506)

As per claims 1, 8 and 15 Kato discloses data transfer control circuit for carrying out data transfer by using a plurality of bus masters, comprising:

- a peripheral apparatus; (col.11, lines 32-46)
- a data bus connected to a peripheral apparatus and including a plurality of unit data buses, (col.3, lines 57-64)
- a plurality of bus masters configured to send a request signal requesting a use of said data bus in unit data bus, and using said data bus in unit data buses requested when a request by means of said request signal is granted; and (col.3, lines 22-30)
- a bus controller configured to split-control said data bus in unit data buses for said plurality of bus masters by giving a grant signal which grants the use of said data bus in units of the unit data bus requested in unit data buses to said bus masters in accordance with an availability of said data

bus in units of the unit data bus, wherein (col.7, lines 34-48), (col.8, lines 4-10)

- the request signal and the grant signal indicate identification or number of the unit data bus divided from the data bus. (col. 11, lines 54-63) wherein the address implies identification)

Kato discloses all the limitations as above except the data bus is divided and through each of which data is transferred concurrently; However, Kenny discloses concurrent data transfers and maximum utilization of available data bus bandwidth is realized by time-slicing the data bus into multiple virtual channels according to a priority multiplexing scheme. (col.3, lines 20-41)

It would have been obvious to one having ordinary skills in the art at the time the invention was made to incorporate Kenny's teaching into Kato's method to have a data bus is divided and through each of which data is transferred concurrently so as that the bus access to i/o devices without incurring additional arbitration-related latencies. (col.2, lines 7-16)

As per claims 2, 9 and 16, Kato discloses bus controller gives the grant signal of the use of said data bus to said bus masters upon receipt of one of a request and release of the use of said data bus in unit data buses inputted from said bus masters. (col.14, lines 26-40)

As per claims 3,10 and 17, Kato discloses bus controller includes a monitor circuit for monitoring the availability of said data bus in unit data buses. (col.8, lines 4-10)

As per claims 4, 11 and 18, Kato discloses bus controller judges whether said data bus is available in unit data busses based on a monitoring result by said monitor circuit, and when said data bus is available, said bus controller gives, the grant signal of the use of said data bus to said bus master. (col.7, lines 34-48)

As per claims 5, 12 and 19, Kato discloses bus controller sends a state signal indicating the availability of said data bus in unit data buses to each of said bus masters based on a monitoring result of said monitor circuit. (col.14, lines 26-40)

As per claims 6, 13 and 20, Kato discloses request signal includes information specifying each unit data bus in said data bus. (col.7, lines 49-62), (col.11, lines 32-63)

As per claims 7 and 14, Kato discloses request signal includes information specifying the number of the unit data buses in said data bus. (col.8, lines 31-40), (col.11, lines 38-60)

As per claim 21, 22, 23, Kato discloses a data transfer control circuit for carrying out data transfer by using a plurality of bus masters, comprising:

- a peripheral apparatus; (col.11, lines 32-37)
- a plurality of bus masters configured to send a request signal requesting a use of said data bus in units of the unit data bus, (col.3, lines 22-30)

- a bus controller configured to split-control said data bus in unit data buses for said plurality of bus masters by giving a grant signal which grants the use of said data bus in units of the unit data bus requested in unit data buses to said bus masters in accordance with an availability of said data bus in units of the unit data bus, wherein (col.7, lines 34-48), (col.8, lines 4-10)
- the request signal and the grant signal are able to specify each of the unit data bus. (col.11, lines 32-63), wherein each address implies specification each of data bus)

Kato discloses all the limitations as above except the data bus is divided and through each of which data is transferred concurrently; However, Kenny discloses concurrent data transfers and maximum utilization of available data bus bandwidth is realized by time-slicing the data bus into multiple virtual channels according to a priority multiplexing scheme. (col.3, lines 20-41)

It would have been obvious to one having ordinary skills in the art at the time the invention was made to incorporate Kenny's teaching into Kato's method to have a data bus is divided and through each of which data is transferred concurrently so as that the bus access to i/o devices without incurring additional arbitration-related latencies. (col.2, lines 7-16)

As per claims 24, 25, 26 Kato discloses a data transfer control circuit for carrying out data transfer by using a plurality of bus masters, comprising:

- a peripheral apparatus; (col.11, lines 32-37)
- a data bus connected to a peripheral apparatus and including a plurality of unit data buses, (col.3, lines 57-64)
- a plurality of bus masters configured to send a request signal requesting a use of said data bus in units of the unit data bus, and using said data bus in unit data buses requested when a request by means of said request signal is granted; and (col.3, lines 22-30)
- a bus controller configured to split-control said data bus in unit data buses for said plurality of bus masters by giving a grant signal which grants the use of said data bus in units of the unit data bus requested in unit data buses to said bus masters in accordance with an availability of said data bus in units of the unit data bus, whereby (col.7, lines 34-48), (col.8, lines 4-10)

Kato discloses all the limitations as above except the memory storing bus arbitration information is accessed concurrently through the unit data bus; However, Kenny discloses concurrent data transfers and maximum utilization of available data bus bandwidth is realized by time-slicing the data bus into multiple virtual channels according to a priority multiplexing scheme. Furthermore, the arbiter selects the next highest priority awaiting for processing and in addition the i/o modules consistently requesting data and each assigned priority, priority is dynamically allocated. (col.3, lines 20-65)

It would have been obvious to one having ordinary skills in the art at the time the invention was made to incorporate Kenny's teaching into Kato's method to have the memory storing bus arbitration information is accessed concurrently through the unit data bus so as that the bus access to i/o devices without incurring additional arbitration-related latencies. (col.2, lines 7-16)

Response to Arguments

3. Applicant's arguments filed on 5/19/03 have been considered but are moot in view of the new ground(s) of rejection.

a. In response to applicant's argument that Kato does not disclose or suggest signal and grant signal for bus arbitration by the bus masters and the bus controller to indicate identification or number of the data bus divided from the data bus. However, Kato does disclose that the bus controller generates a first bus request signal sent to the bus arbitrator according to the bus area select from address decoder and furthermore the controller asserts the bus request until it receives grant signal from bus arbitrator which all implies identification. (see col. 11, lines 38-62)

Conclusion

4. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kim Huynh whose telephone number is (703)305-5384 or via e-mail addressed to [kim.huynh3@uspto.gov]. The examiner can normally be reached on M-F 8:30AM- 6:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on (703) 305-4815 or via e-mail addressed to [mark.rinehart@uspto.gov]. The fax phone numbers for the organization where this application or proceeding is assigned are (703)746-7249 for regular communications and (703)746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)306-5631.

Kim Huynh

July 20, 2003